UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,878	10/07/2003	Gang Xue	02-1059-A	6424

20306 7590 04/05/2006

MCDONNELL BOEHNEN HULBERT & BERGHOFF LLP
300 S. WACKER DRIVE
32ND FLOOR
CHICAGO, IL 60606

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,878	XUE ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,12-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 16* is/are allowed.

6)☒ Claim(s) *1-7,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 0120* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

DETAILED ACTION

1. Applicant's amendment filed March 09, 2006 has been entered. Claims 1 and 12 have been amended.

2. Claims 1 – 7, 12 – 14, and 16 are pending.

Response to Arguments

3. Applicant's arguments filed March 09, 2006 have been fully considered but they are not persuasive.

In view of the claims amendment, applicants are requested to consider the following, which establishes grounds for the claim rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 7, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Bude et al. (US Pat 6,528,845 B1).

Regarding **claims 12 and 13**, Bude et al. disclose a memory circuit comprising:

an array of single bit nonvolatile memory cells (fig. 1 shows a single bit nonvolatile memory cell 100, which is inherently exemplary for an array of identical cells in memory art), each of the memory cells comprising a semiconductor substrate (110) including a bulk region (120), a source (130), a drain (140), and a channel in the bulk region and in between the source and the drain (region in 120 and in between 130 and 140); and a control gate that comprises a control gate electrode (170) and a dielectric stack (stack of layers 150, 160, and 190), the dielectric stack consisting of one or more dielectric layers (150 and 190 made of SiO_2 and 160 made of SiN, col. 4, lines 1 – 27), wherein at least one of the one or more dielectric layers is a charge storage dielectric layer (layer 160 made of Silicon Nitride, which is a charge trapping insulator layer);

peripheral circuitry (the memory circuit inherently includes a peripheral circuitry in order to effect programming, erasing, and/or reading of the memory cells with specific voltage biases as disclosed in col. 4, lines 50 – 63, and col. 5, line 45 – col. 6, line 2. further, the peripheral circuitry must generate an on-chip voltage in order to supply to the memory cells, which are on-chip), the peripheral circuitry coupled with the memory cell such that programming of each memory cell is effected using voltage having absolute values of 5V or less (col. 4, lines 51 – 60, all given voltage biases have absolute value of 5V or less),

wherein the memory cells are programmed as a result of injection of hot carriers from the bulk region near the drain of the memory cell (fig. 3, col. 4, line 64 – col. 5, line 10, in which lines 8 – 10 of col. 5 describes the first impact ionization of hot carriers—electrons from the source 140 from the bulk region, in the channel, near the drain of the memory cell—accelerated toward the drain region 140 in the field 311), a majority of the injected hot carriers being (i) generated by a secondary impact ionization mechanism (col. 5, lines 10 – 14, secondary impact ionization caused by the holes within the tub 120 and accelerates the resulting electrons toward the substrate 110 surface and the oxide layer 150 near the drain by vertical filed 313), (ii) injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer (col. 5, lines 14 – 21, "..., those electrons can be trapped in a localized region 320 of the trap charge layer 150 near the drain region 140").

Regarding **claim 1**, Bude et al. also disclose a method for programming a single bit nonvolatile memory cell on a metal-dielectric semiconductor technology chip (see above), wherein the method of programming comprises:

applying a first voltage having a first polarity to the drain (col. 4, lines 58 – 59, "... Vds ranges from about 1.8 volts to about 3.0 volts..."—drain potential with respect to source potential having positive value),

applying a second voltage of the first polarity to the control gate electrode (col. 4, lines 57 – 58, "... Vgs ranges from about 1.8 volts to 3.0 volts..."—gate potential with respect to source potential having positive value, which means the drain and the control gate electrode are applied with voltages of same polarity—first polarity); and

applying a third voltage having a second polarity opposite to the first polarity to the bulk (col. 4, lines 59 – 60, "Vts ranges from about –0.5 to about –3.0 volts". Tub voltage Vt with respect to source potential Vs having negative values, which is opposite to the first polarity; and

applying electrical ground to the source (col. 4, lines 60 – 61, "Furthermore, in a preferred embodiment, Vs is about zero ...". Vs being source voltage).

Regarding **claim 2**, see grounds for the rejection of claim 12 and 13 above.

Regarding **claim 3**, given the voltage ranges as indicated in col. 4, lines 55 – 61, if Vds is 3.0 volts and Vgs is 1.8 volts, the difference of absolute values of these voltages is less than 1.5 volts.

Regarding **claim 4**, if Vgs is 3.0 volts and Vts is –3.0 volts, the effective gate to bulk voltage applied by the second and third voltage is 6 volts, which is more than 4V.

Regarding **claim 5**, the absolute values of each of the second and third voltages are 5V or less (see above claims 2, 12, and 13).

Regarding **claim 6**, the charge storage dielectric layer 160 is positioned between oxide layers 150 and 190.

Regarding **claim 7**, the charge storage dielectric layer comprises nitride (160 made of Silicon Nitride. See above).

Allowable Subject Matter

6. **Claims 14 and 16** are allowed.

7. The examiner's statement of reasons for allowance was provided in the Office Action, mailed on August 12, 2005.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D. Pham
March 23, 2006

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800